

Amendments to the Specification

Please insert the paragraph shown below after the paragraph beginning on page 7, line 8.

Fig. 6c depicts a partial cross-sectional view of the microelectronic topography depicted in Fig. 6a taken along line BB;

Fig. 6d depicts an alternative partial cross-sectional view of the microelectronic topography depicted in Fig. 6a taken along line BB;

Please replace the paragraph beginning on page 17, line 18, with the following rewritten paragraph.

As shown in Fig. 4, read transistor 27 and program transistor 29 may be arranged within word lines 34 and 32, respectively. Accordingly, read transistor 27 may be adapted to enable current flow through conductive path 41 by the application of a sufficient voltage along word line 34. In addition, program transistor 29 may be adapted to enable current flow through conductive path 43 adjacent to magnetic cell junction 25 upon an application of a sufficient voltage to word line 34. The configuration of read transistor 27 and program transistor 29 is opposite to the arrangement of read transistor 26 and program transistor 28 in memory cell 22a in which transistors 26 and 28 are configured to enable current flow upon the application of voltages to word lines 32 and 34, respectively. As a consequence, memory array 54 includes two separate ground lines for read transistors 26 and 27. In particular, memory array 54 may include ground line 30 coupled to read transistor 26 and ground line 58 coupled to read transistor 27. In some embodiments, read transistors 26 and 27 may be coupled to a common ground line such that the number of ground lines within memory array 54 may be minimized. For example, read transistor 27 may be coupled to ground line 30 instead of ground line 58 as shown by dashed line 45 in Fig. 4, indicating an alternative embodiment of read transistors 27 and 29 coupled to the same ground line. In yet other embodiments, read transistors 27 and 29 may be alternatively coupled to ground line 58. ~~Consequently, in some cases, ground lines 30 and 58 may signify the same line but are drawn as separate lines in Fig. 4 to simplify the illustration of the drawing. In yet other embodiments ground lines 30 and 58 may be separate.~~

Please replace the paragraph beginning on page 22, line 1, with the following rewritten paragraph.

Figs. 6a-6c illustrate an exemplary configuration of conductive structures arranged about magnetic cell junction 24 which may constitute conductive paths 38 and 40 of memory arrays 20, 52 or 54. In particular, Fig. 6a illustrates a partial top view of microelectronic topography 68 having a configuration of conductive structures coupled to bit line BL0 and arranged adjacent to magnetic cell junction 24. Fig. 6b illustrates a partial cross-sectional view of microelectronic topography 68 taken along line AA of Fig. 6a and Fig. 6c illustrates a partial cross-sectional view of microelectronic topography 68 taken along line BB of Fig. 6a. An alternative configuration of the structures which may be configured within microelectronic topography 68 is shown in Fig. 6d, specifically with conductive structure 70 spaced apart from magnetic cell junction 24 by via 71. Such an alternative configuration of conductive structure 70 with respect to magnetic cell junction 24 may be applied to other views of microelectronic topography 68 (similar to those shown for Figs. 6a and 6b, for example), but have not been illustrated for the sake of brevity. In general, the configurations depicted in Figs. 6a-~~6c~~6d may be employed within memory array 20, 52 or 54. As such, Figs. 6a-~~6c~~6d are not necessarily restricted to one embodiment of the memory array described herein.

Please replace the paragraph beginning on page 22, line 12, with the following rewritten paragraph.

As shown in Figs. 6a-~~6c~~6d, microelectronic topography 68 may include conductive structures 70 and 72, vias 74, 76 and 78 and electrode 80. In particular, magnetic cell junction 24 may be interposed between conductive structure 70 and electrode 80, which is in turn coupled to via 78 as shown in Figs. 6c and 6d. Via 78 may be coupled to additional conductive structures which couple to read transistor 26 of memory cell 22a. In this manner, conductive structure 70, magnetic cell junction 24, electrode 80, via 78 and the other conductive structures coupled to read transistor 26 may constitute conductive path 38. In particular, current induced from an application of voltage to bit line BL0 may travel through such structures for a read operation of the memory cell. For such a configuration, conductive structure 70 is preferably arranged in contact with magnetic cell junction 24 as shown in Fig. 6c such that the current may be conducted therethrough. In other embodiments, however, conductive structure 70 may be spaced above magnetic cell junction 24 and coupled thereto by a via, such as shown in Fig. 6d.

Please replace the paragraph beginning on page 23, line 9, with the following rewritten paragraph.

It is noted that the series of conductive structures constituting conductive path 40 may be altered from the ~~illustration~~ illustrations depicted in Figs. 6a-~~6c~~6d. For example, in some embodiments, conductive structure 70 extending from bit line BL0 may be aligned with the lower side of magnetic cell junction 24 and conductive structure 72 may be aligned with the upper side of magnetic cell junction 24. In such an embodiment, the arrangement of via 74 and 76 may be altered such that conductive path 40 may run under and then above magnetic cell junction 24 down to a program transistor arranged below. Conductive structure 72, in such an embodiment, may be arranged in contact with the cell junction and, therefore, may serve as part of conductive path 38 in some cases. In either case, conductive structures 70 and 72 may, in some embodiments, be arranged such that conductive path 40 passes magnetic cell junction 24 in two distinct segments. Such an arrangement of structures is described in more detail below and is referred to interchangeably herein as a "loop around" or "fold back" configuration.

Please replace the paragraph beginning on page 23, line 23, with the following rewritten paragraph.

Although the description of conductive path 40 below is described in reference to the fold back configuration of conductive structures 70 and 72 around magnetic cell junction 24, conductive path 40 of the memory arrays described herein may, in some embodiments, include a series of conductive structures which do not loop around the cell junction. In particular, conductive path 40 may, in some embodiments, include one or more conductive structure arranged along one side of magnetic cell junction 24 and may be substantially absent of structures along the opposing side of the cell junction. An exemplary configuration of conductive path 40, in such an embodiment, may include conductive structure 70 arranged adjacent to magnetic cell junction 24 as shown in Figs. 6a-~~6c~~6d. The position of conductive structures 72 and 76, however, may be modified such that the conductive path within the series of structures continues downward from via 74 without being arranged in close enough proximity to magnetic cell junction 24 to induce a magnetic field which may affect the junction's magnetic state. Alternatively, conductive structure 72 may be arranged adjacent to magnetic cell junction 24 as shown in Figs. 6a-~~6c~~6d and the position of conductive 70 may be altered such that a magnetic field induced therefrom does not affect the magnetic state of magnetic cell junction 24. The magnitude of magnetic fields generated from memory arrays including such non-fold back

configurations are discussed in more detail below relative to the magnitude of magnetic fields generated from memory arrays with the fold back arrangement. In addition, the voltage requirements of memory arrays including non-fold back configurations are discussed in more detail below relative to memory arrays with the fold back arrangement.

Please replace the paragraph beginning on page 25, line 28, with the following rewritten paragraph.

In some cases, the magnitude of the magnetic field induced by the arrangement of conductive structures 70 and 72 may be sufficient to set and/or change the direction of magnetic vectors within magnetic cell junction 24 such that a particular bit value may be stored therein. Consequently, in some embodiments, the inclusion of a digit line in microelectronic topography 68 may not be necessary to identify a selected memory cell and, therefore, may be omitted as shown in Figs. 6a-6c6d. Consequently, the write selectivity of a memory array with a fold-back or loop around configuration of conductive structures around magnetic cell junction 24 may be increased or negated relative to the write selectivity of a conventional memory array with cross-hatched configuration of bit and digit lines. As a result, the reliability of a memory array having a fold-back or loop around pattern of conductive structures around a magnetic cell junction may be greater than an array having a conventional configuration of cross-hatched bit and digit lines. In an alternative embodiment, digit lines may be included within microelectronic topography 68 to aid in selecting a particular memory cell for a write operation of the array.

Please replace the paragraph beginning on page 28, line 24, with the following rewritten paragraph.

In addition, it is noted that although the description of manipulating logic states within magnetic junction 24 is directed at elliptically shaped magnetic junctions, other shapes known in the MRAM fabrication industry may also or alternatively be used to promote easy and hard axes orientations within magnetic layers of cell junctions. Therefore, although configuration of memory cell 22a is sometimes described in reference to the elongated and shortened dimensions magnetic cell junction 24, the configuration of memory cell 22a is not restricted to such dimensions of the magnetic cell junction. In fact, in some embodiments, magnetic cell junctions 26a and 26b may not include elongated or shortened dimensions. Consequently, the ~~embodiment~~ embodiments depicted in Figs. 6a-6c-6d ~~is~~are not restricted to elliptically shaped

magnetic cell junctions. In particular, the magnetic memory array configuration described herein may be incorporated with magnetic cell junctions of any shape and/or size.

Please replace the paragraph beginning on page 29, line 7, with the following rewritten paragraph.

In general, magnetic vectors existing within an equilibrium state of a layer (i.e., when no external energy is applied) may be more easily changed with a magnetic field which is not directly parallel with the magnetic vectors. Consequently, it is generally desirable to induce a magnetic field which is not aligned with the easy axis of the junction in order to alter the overall magnetization direction of the magnetic cell junction from its equilibrium state. As such, it may be advantageous to orient magnetic cell junction 24 and/or conductive structures 70 and 72 such that a magnetic field induced by conductive structures 70 and 72 is not directed along the easy axes of magnetic cell junction 24. For example, magnetic cell junction 24 may be oriented to have an easy axis (e.g., an elongated dimension) arranged at an angle between approximately 0° and approximately 90° relative to the parallel arrangement of conductive structures 70 and 72 as shown in ~~Figs. 6a-6c~~ Fig. 6a. In some cases, conductive structures 70 and 72 may be additionally or alternatively oriented in a non-parallel manner such that an aggregate magnetic field induced therefrom is not aligned with an easy axis of magnetic cell junction 24.

Please replace the paragraph beginning on page 29, line 22, with the following rewritten paragraph.

As shown in Fig. 6a, ~~conductor~~ conductive structure 70 may be configured as an extension of bit line BL0 in some embodiments. In such a case, bit line BL0 may include a plurality of extensions each extending over a different magnetic cell junction within a column of the memory array. In this manner, bit line BL0 may serve as a global bit line to a single column of magnetic cell junctions. In other embodiments, bit line BL0 may further include extensions on its opposing side such that conductive structures extend over magnetic cell junctions within another column of the array. In such embodiments, bit line BL0 may serve as a global bit line to a plurality of magnetic cell junctions arranged within two columns of the array. In some cases, conductive structure 70 may be a distinct structure from bit line BL0. In particular, conductive structure 70 may be spaced apart from bit line BL0 and coupled thereto by a via. An exemplary embodiment of such a configuration is described in reference to Figs. 7a-7c. In either case,

conductive structures 70 and/or 72 may include a cladding layer configured to shield the structures such that other magnetic fields generated within the array do not affect the magnetic fields generated by structures 70 and/or 72. Such an inclusion of cladding layers may be particularly advantageous in embodiments in which bit line BL0 is arranged in close proximity with conductive structure 70. In yet other embodiments, bit line BL0 may be spaced far enough away such that conductive structures 70 and 72 may not need cladding layers.

Please replace the paragraph beginning on page 30, line 21, with the following rewritten paragraph.

In general, the arrangement of structures within microelectronic topography 82 may be similar to the arrangement of structures within microelectronic topography 68 of Figs. 6a-6e-6d which share the similar respective reference numbers. For example, microelectronic topography 82 may include magnetic cell junction 24, conductive structures 70 and 72, vias 74, 76, and 78 and electrode 80. In addition, microelectronic topography 82 may include conductive structure 70 directly in contact or spaced apart from magnetic cell junction 24 as similarly shown in Figs. 6c and 6d, respectively, for microelectronic topography 68. As shown in Figs. 7b and 7c, magnetic cell junction 24 may be interposed between conductive structure 70 and electrode 80, which may in turn be coupled to via 78. In general, via 78 may be coupled to additional conductive structures which couple to read transistor 26 of memory cell 22a. In this manner, conductive structure 70, magnetic cell junction 24, electrode 80, via 78 and the other conductive structures coupled to read transistor 26 may constitute conductive path 38. Fig. 7b depicts an alternate view of microelectronic topography 82 to show conductive structures 70 and 72 connected by via 74. Fig. 7b further illustrates conductive structure 72 coupled to via 76, which may be coupled to one or more other conductive structures coupled to program transistor 28 of memory cell 22a. Such an arrangement of conductive structures may constitute conductive path 40.